REMARKS

I. Present Disposition of the Claims

The Applicants wish to reiterate thanks to the Examiner for the useful comments in the Telephonic Interview on April 23, 2003, and the non-final Office Action mailed April 9, 2003, that was received on April 15, 2003. The Specification has been herein amended. Independent Claims 1, 6, 11, and 16 have been herein amended and dependent Claims 5 and 15 are herein canceled, without prejudice, to better encompass the full scope and breadth of the present invention, notwithstanding the Applicants' belief that the claims were allowable as originally filed.

Specifically, independent Claims 1 and 11 are herein amended by inserting respectively the limitations from herein canceled dependent Claims 5 and 15 and by adding the additional limitation that the presently recited reduced-oxygen Cu-Zn alloy fill has a uniform zinc distribution (Specification, p. 11, ll. 29-30). Therefore, reconsideration of the present application in light of the foregoing proposed amendment and these remarks is respectfully requested.

II. Rejection of Claims 1-6 and 10-16 under 35 U.S.C. § 103(a)

The Examiner has rejected Claims 1-6 and 10-16, under 35 U.S.C. § 103(a), as being unpatentable over Krishnamoorthy et al. (US 6,486,533) ("Krishnamoorthy"), in view of Miyafuji et al. (US 6,313,064) ("Miyafuji"), stating:

> In re claim 1, Krishnamoorthy et al. teach the claimed method of fabricating a semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, comprising the steps of:
> - providing a semiconductor substrate having a Cu surface 35 (i.e. a bonding layer; col. 4, lines 60-64) formed in a via (Fig. 1);
> - providing a chemical solution (i.e. an electroplating solution);
> - electroplating the Cu surface 35 in the chemical solution, thereby forming a Cu-Zn alloy 40 fill in the via and on the Cu surface 35 in the chemical solution, thereby
> - rinsing the Cu-Zn alloy fill 40 in a solvent stored in a rinsing chamber (col. 9, lines 33-37)
> - drying the Cu-Zn fill 40 under a gaseous flow (col. 9, lines 33-44);
> - annealing the Cu-Zn alloy fill 40 formed in the via and on the Cu surface 35 (col. 5, line 61 and col.6, line 6), thereby forming a post-annealed Cu-Zn alloy fill;
> - planarizing the post-annealed Cu-Zn alloy fill and the Cu surface 35, thereby completing formation of the post-annealed Cu-Zn alloy filled dual-inlaid interconnect structure (Fig.1); and
> - completing formation of the semiconductor device.
>
> Krishnamoorthy et. al. is silent as to the post-annealed Cu-Zn alloy being the claimed reduced-

oxygen Cu-Zn alloy.

Pending independent Claims 1 and 11 are herein amended, as discussed supra, and dependent Claims 2, 3, 4, 6, 10, 12, 13, 14 and 16 respectively subsume the limitations of the independent claims from which they depend. Dependent Claims 5 and 15 are herein canceled, without prejudice, as discussed supra, thereby rendering moot the Examiner's ground for their rejection on this basis.

Notwithstanding independent Claims 1 and 11 being herein amended, the Applicants respectfully hereby traverse the Examiner's ground for rejection on this basis. Contrary to the present invention, Krishnamoorthy teaches a method for forming microelectronic metallized structures wherein a dielectric layer 25 provides a foundational layer for depositing an ultra-thin film bonding layer 35 and a low-Me concentration, copper-zinc, alloy layer 40. Specifically, Krishnamoorthy recites "[a] metallized structure 20 is comprised of an ultra-thin bonding layer 35 disposed exterior to the dielectric layer 25, a low-zinc concentration, copper-zinc alloy layer 40 disposed exterior to the ultra-thin bonding layer 35, and an optional primary conductive layer 45 disposed exterior to the copper-zinc layer 40" (Col. 4, ll. 30-42; Exhibit B). The dielectric layer is the foundational layer for the Krishnamoorthy metallization scheme (Col. 4, ll. 13-27):

> The composition of the dielectric layer 25 is generally dependent on the function of the metalization structure 20. When the metalization structure 20 is used to implement a post or line of an electrical interconnect network, the dielectric layer 25 is preferable comprised of a low-K material. When the metalization structure is used to implemcnt a discrete microelectronic component such as a capacitor, however, the dielectric layer 25 is preferably comprised of a high-K material. To increase adhesion between the dielectric layer 25 and a subsequent layer, such as ultra-thin bonding layer (35), the surface of the dielectric layer may be subject o an adhesion promoting process. For example, the dielectric layer surface may be subject to treatment in an atmosphere having a high ozone content. Alternatively, some form of mild mechanical or chemical abrading process may be used.

Stated differently, the metallization structure described in Krishnamoorthy requires a **specific dielectric, i.e., non-electrically conductive or insulating, foundational material layer**, as exemplified in the above duplicated passage. Further,"**[t]he bonding layer 35 functions principally as an adhesion promoter** to bond the copper-zinc alloy layer 40 to the dielectric layer 25" (Col. 4, ll. 47-50). At best, Krishnamoorthy teaches, if desired, a primary conductor, such as a film of copper, may be formed exterior to the foregoing layer sequence. Thus, after the above described Krishnamoorthy layer sequence, i.e., including dielectric layer

25 and bonding layer 37, an additional copper film layer may be deposited on the exterior, **while in the presently claimed invention, the first step in metallization process is Cu.** Further, **the present invention** does not require a bonding layer 35 or a dielectric layer 25, permitting the presently claimed **direct depositing of electrically conductive interim Cu-Zn alloy on a Cu surface 20.** Thus, independent Claim 1 of the present invention is not taught, suggested, nor motivated by Krishnamoorthy.

Along with Krishnamoorthy, Miyafuji merely teaches that "[w]hen **[a] copper alloy** containing zinc is oxidized, zinc, as well as titanium, is **preferentially oxidized** so that an oxide which mainly **contains ZnO is produced in it surface layer**" (col. 4, ll. 8-11). When the zinc oxide is **irradiated with ultraviolet light rays**, the oxide **exhibits an optical catalyst function,** in the same way that TiO_2 does to create an antibacterial effect which is a solution to a problem which is entirely dissimilar to the problems sought to be solved by the present invention. The Examiner asserts:

> ... one of ordinary skill in the art would have recognized post annealed Cu-Zn alloy is nothing but the reduced-oxygen Cu-Zn alloy, in light of the teachings of Miyafuji et al.. In particular, Miyafuji et al. in an analogous art of Cu-Zn alloy formation suggest that by subjecting the Cu-Zn alloy to a heat treatment (i.e. the annealing) at the proper temperature the Zn in the Cu-Zn would oxidize as ZnO due to the fact that Zn has far more intense affinity with oxygen than Cu. In other words, by subjecting to the heat treatment (i.e. the annealing) oxygen concentration in the Cu-Zn alloy would reduce, i.e. producing the reduced-oxygen Cu-Zn alloy [Office Action mailed 04/09/2003, p. 3, ll. 7-13].

However, Miyafuji merely teaches "[i]n order to oxidize titanium, silicon, or zinc for the copper alloy of the present invention, heat treatment may be conducted in the air or in [the] vacuum ..." (Col. 4, ll. 57-62; Exhibit C). Further, Miyafuji teaches "[s]ince these elements have far more intense affinity with oxygen (standard free energy for the production of oxides) than copper, they can be preferentially oxidized. Oxygen is diffused into the copper alloy, and thus the alloy can be industrially produced in such a manner that the amount or size of the produced oxides, the depth of the oxidized layer, and the like are controlled by combining heating atmosphere (oxygen partial pressure), heating temperature and heating time appropriately" (Col. 4, ll. 63-68; Col. 5, ll. 1-5; Exhibit C). In other words, Krishnamoorthy, in view of Miyafuji, **creates oxide particles of various diameters, depending on the diffusion depth of the**

oxygen. For example, Fig. 1 (Exhibit C) **shows titanium oxide particles at the surface larger than titanium oxide particles at a depth below the surface** (Fig. 1, Exhibit C). In contrast, the present invention positively recites a method, including the steps of rinsing and drying the substrate, for **the production of a reduced-oxygen Cu-Zn alloy fill 30 having a uniform zinc distribution**, as indicated by block 2006 (Specification, p. 11, ll. 29-30).

Thus, Krishnamoorthy, even in view of Miyafuji, does not teach, motivate, nor suggest herein amended independent Claims 1 and 11, respectively reciting:

1. **(currently amended)** A method of fabricating a semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, comprising the steps of:
providing a semiconductor substrate having a Cu surface formed in a via;
providing a chemical solution;
electroplating the Cu surface in the chemical solution thereby forming said a Cu-Zn alloy fill in the via and on the Cu surface,
wherein said electroplating comprises using an electroplating apparatus,
wherein said electroplating apparatus comprises:
(a) a cathode-wafer;
(b) an anode;
(c) electroplating vessel; and
(d) a voltage source, and
wherein said cathode-wafer comprises a Cu surface,
rinsing the Cu-Zn alloy fill in a solvent;
drying the Cu-Zn alloy fill under a gaseous flow;
annealing the Cu-Zn alloy fill formed in the via and on the Cu surface, thereby forming **a reduced-oxygen Cu-Zn alloy fill having a uniform zinc distribution;**
planarizing the reduced-oxygen Cu-Zn alloy fill and the Cu surface, thereby completing formation of a reduced-oxygen Cu-Zn alloy filled dual-inlaid interconnect structure; and
completing formation of the semiconductor device.

11. **(currently amended)** A semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, fabricated by a method comprising the steps of:
providing a semiconductor substrate having a Cu surface formed in a via;
providing a chemical solution;
electroplating the Cu surface in the chemical solution, thereby forming a Cu-Zn alloy fill in the via and on the Cu surface;
wherein said electroplating comprises using an electroplating apparatus,
wherein said electroplating apparatus comprises:
(a) a cathode-wafer;
(b) an anode;
(c) electroplating vessel; and
(d) a voltage source, and
wherein said cathode-wafer comprises a Cu surface,
rinsing the Cu-Zn alloy fill in a solvent;

drying the Cu-Zn alloy fill under a gaseous fl w;
annealing the Cu-Zn alloy fill formed in the via and on the Cu surface, thereby forming a **reduced-oxyg n Cu-Zn alloy fill having a unif rm zinc distribution;**
planarizing the reduced-oxygen Cu-Zn alloy fill and the Cu surface, thereby completing formation of a reduced-oxygen Cu-Zn alloy filled dual-inlaid interconnect structure; and
completing formation of the semiconductor device.

As such, Krishnamoorthy, even in view of Miyafuji, does not teach, motivate, nor suggest the dependent Claims 2, 3, 4, 10, 12, 14, and 16, now subsuming the limitations of the herein amended independent Claims 1 and 11. Therefore, the Applicants respectfully request that the Examiner's grounds for rejection on this basis be withdrawn.

II. Rejection of Claims 1, 2, 4-7, 11, 12 and 14-17 under 35 U.S.C. § 103(a)

The Examiner has rejected Claims 1, 2, 4-7, 11, 12, and 14-17, under 35 U.S.C. § 103(a), as being unpatentable over Chen et al. (US 2002/008034 A1) ("Chen"), in view of Miyafuji et al. (US 6,313,064) ("Miyafuji"), stating:

In re claim 1, Chen et. al. teach the claimed method of fabricating a semiconductor device, having a reduced-oxygen copper zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, comprising steps of;

- providing a semiconductor substrate having a Cu surface 15 (i.e. a copper seed layer) formed in a via 5 (Fig. 2B);
- providing a chemical solution (i.e an electroplating solution);
- electroplating the Cu surface 15 in a chemical solution, thereby forming a Cu-Zn alloy 18 fill in the via 5 and on the Cu surface 15 (Fig. 2C and paragraph [0067]);
- rinsing the Cu-Zn alloy fill in a solvent (paragraphs [0082] and [0179]);
- drying the Cu-Zn alloy fill under a gaseous flow (paragraphs [0082] and [0179]);
- annealing (via a thermal processing step) the Cu-Zn alloy fill 18 formed in the via 5 and on the Cu surface 15 (paragraphs [0069] and [0094], thereby forming a post -annealed Cu-Zn alloy fill;
- planarizing the post-annealed Cu-Zn alloy fill and the Cu surface 15, thereby completing formation of the post-annealed Cu-Zn alloy filled dual-inlaid interconnect structure (Figs. 2D-2E); and
- completing formation of the semiconductor device.

Chen et al. is silent as to the post-annealed Cu-Zn alloy being the claimed reduced-oxygen Cu-Zn alloy.

Pending independent Claims 1 and 11 are herein amended, as discussed supra, and dependent Claims 2, 4, 6, 7, 12, 14 and 16 subsume the limitations of the independent claims from which they depend. Dependent Claims 5 and 15 are herein canceled, without prejudice, as

discussed supra, thereby rendering moot the Examiner's ground for their rejection on this basis.

Notwithstanding independent Claims 1 and 11 are being herein amended, the Applicants respectfully traverse the Examiner's ground for rejection on this basis. Contrary to the present invention, Chen teaches "a semiconductor workpiece, such as a semiconductor wafer 30, is positioned face down in a bath 35 of electroplating solution" (Para. 0070). Further, Chen teaches "[o]ne or more contacts 40 are provided to connect the wafer 30 to a plating power supply 45 as a cathode of an electroplating cell" (Para. 0070; Exhibit D). An anode 50 is disposed in the bath 35 and is connected to the plating power supply 45 (Para. 0070). Thus, Chen teaches electroplating a wafer seed using contacts 40, acting as cathodes, which contact one or more locations along the edges of the semiconductor wafer 30. In contrast, the present invention comprises a cathode-wafer surface (i.e., Specification, p. 4, l. 11) which receives an **equal potential voltage distribution** across the entire semiconductor wafer while being submerged **in the electroplating bath** (Fig. 7; Exhibit A). Thus, the present invention method of electroplating Cu-Zn alloy is not taught, suggested nor motivated by Chen.

As discussed above, Miyafuji, does not teach, motivate, nor suggest the present invention method, comprising the steps of rinsing and drying the substrate, for **the production of a reduced-oxygen Cu-Zn alloy fill 30 having a uniform zinc distribution**, as indicated by block 2006 (Specification, p. 11, ll. 29-30). Similar to Krishnamoorthy, Chen, even in view of Miyafuji, **creates oxidized electroplated metal particles whose size depends on the diffusion depth of the oxygen.** For example, Miyafuji **shows titanium oxide particles formed at the surface are larger than titanium oxide particles formed a depth below the surface** (Fig. 1, Exhibit C).

Thus, Chen, even in view of Miyafuji, does not teach, motivate, nor suggest herein amended independent Claims 1 and 11, respectively reciting:

> 1. **(currently amended)** A method of fabricating a semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, comprising the steps of:
> providing a semiconductor substrate having a Cu surface formed in a via;
> providing a chemical solution;
> electroplating the Cu surface in the chemical solution thereby forming said a Cu-Zn alloy fill in the via and on the Cu surface,
> wherein said electroplating comprises using an electroplating apparatus,
> wherein said electroplating apparatus comprises:
> (a) a cathode-wafer;

(b) an anode;
(c) electroplating vessel; and
(d) a voltage source, and
wherein said cathode-wafer comprises a Cu surface,
rinsing the Cu-Zn alloy fill in a solvent;
drying the Cu-Zn alloy fill under a gaseous flow;
annealing the Cu-Zn alloy fill formed in the via and on the Cu surface, thereby forming **a reduced-oxygen Cu-Zn alloy fill having a uniform zinc distribution;**
planarizing the reduced-oxygen Cu-Zn alloy fill and the Cu surface, thereby completing formation of a reduced-oxygen Cu-Zn alloy filled dual-inlaid interconnect structure; and
completing formation of the semiconductor device.

11. **(currently amended)** A semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, fabricated by a method comprising the steps of:
providing a semiconductor substrate having a Cu surface formed in a via;
providing a chemical solution;
electroplating the Cu surface in the chemical solution, thereby forming a Cu-Zn alloy fill in the via and on the Cu surface;
wherein said electroplating comprises using an electroplating apparatus,
wherein said electroplating apparatus comprises:
(a) a cathode-wafer;
(b) an anode;
(c) electroplating vessel; and
(d) a voltage source, and
wherein said cathode-wafer comprises a Cu surface,
rinsing the Cu-Zn alloy fill in a solvent;
drying the Cu-Zn alloy fill under a gaseous flow;
annealing the Cu-Zn alloy fill formed in the via and on the Cu surface, thereby forming **a reduced-oxygen Cu-Zn alloy fill having a uniform zinc distribution;**
planarizing the reduced-oxygen Cu-Zn alloy fill and the Cu surface, thereby completing formation of a reduced-oxygen Cu-Zn alloy filled dual-inlaid interconnect structure; and
completing formation of the semiconductor device.

As such, Chen, even in view of Miyafuji, does not teach, motivate, nor suggest the dependent Claims 2, 4, 6, 7, 12, 14, 16, and 17, now subsuming the limitations of the herein amended independent Claims 1 and 11. Therefore, the Applicants respectfully request that the Examiner's grounds for rejection on this basis be withdrawn.

II. Rejection of Claims 8, 9, 18 and 19 under 35 U.S.C. § 103(a)

The Examiner has rejected Claims 8, 9, 18, and 19 under 35 U.S.C. § 103(a), as being unpatentable over Chen et al. (US 2002/008034 A1) ("Chen"), in view of Miyafuji et al. (US 6,313,064) ("Miyafuji"), and in further view of Dublin et al. (US 2002/0084529),

stating:

> However, Dublin et al. in analog us art (Fig. 6) teach steps of :(1) forming a barrier layer 240 in a via; (2) forming an underlying layer 280A (i.e. a shunt material layer) comprising tin on the barrier layer 240 (paragraphs [0039] and [0031]); (3) forming a Cu surface 290 (i.e. copper seed layer) over the barrier layer 240 and on the underlying layer 280A; and (4) forming an electroplated Cu-Zn alloy 260 on the Cu surface 290.

Since Claims 8, 9, 18, and 19 are all dependent claims, they are herein only constructively amended by respectively subsuming the limitations of herein amended independent Claims 1 and 11 as discussed, supra.

Notwithstanding independent Claims 1 and 11 being herein amended, the Applicants respectfully traverse the Examiner's ground for rejection on this basis. **Dublin** merely teaches "interconnect material 260 is copper or a copper alloy such as the alloy may be plated or the copper introduced and doped" (Para. 0042). In addition, Dublin teaches "the introduction of interconnect material 260 of, for example, copper or a copper alloy, structure 200 may be planarized, if necessary, by for example, a chemical-mechanical polish to expose the dielectric material 230 and to define the interconnect structures (Para. 0042; Fig. 4; Exhibit E). Chen, even in view of Miyafuji, and even in further view of Dublin, does not teach, motivate, nor suggest the present invention, because the Chen substrate metallization plating bath, as shown in Exhibit D, combined with the substrate oxidation processing in Miyafuji, as shown in Exhibit C, would create non-uniform diameter oxidized metal particles, as discussed supra, where the particle dimensionality is a function of its depth below the surface. Further, combining particle annealing with Dublin's subsequent substrate annealing would only "... improve the adhesion of the seed material 290 to a subsequently introduced interconnect material" (Para. 0041). In contrast, the present inventive process steps, including annealing the surface, decreases electromigration through decreasing drift velocity of the particles during line metalization, resulting in a uniform distribution of zinc in the layer (Specification, p. 3, ll. 23-27).

Thus, Chen, even in view of Miyafuji, and even in further view of Dublin, does not teach, motivate, nor suggest the herein constructively amended dependent Claims 8, 9, 18, and 19, respectively reciting:

> 8. **(original)** A method, as recited in Claim 7,
> wherein said semiconductor substrate further comprises an underlayer formed

on the barrier layer,
wherein said underlayer comprises at least one material selected fr m a group consisting essentially of tin (Sn) and palladium (Pd), and
wherein said Cu surface is formed over said barrier layer and on said underlayer.

9. **(original)** A method, as recited in Claim 8,
wherein said underlayer comprises a thickness range of approximately 15 Å to approximately 50 Å,
wherein said barrier layer comprises a thickness range of approximately 30 Å to approximately 50 Å,
wherein said Cu surface comprises a thickness range of approximately 50 Å to approximately 70 Å, and
wherein said Cu-Zn alloy fill comprises a thickness range of approximately 300 Å to approximately 700 Å.

18. **(original)** A device, as recited in Claim 17,
wherein said semiconductor substrate further comprises an underlayer formed on the barrier layer,
wherein said underlayer comprises at least one material selected from a group consisting essentially of tin (Sn) and palladium (Pd), and
wherein said Cu surface is formed over said barrier layer and on said underlayer.

19. **(original)** A device, as recited in Claim 18,
wherein said underlayer comprises a thickness range of approximately 15 Å to approximately 50 Å,
wherein said barrier layer comprises a thickness range of approximately 30 Å to approximately 50 Å,
wherein said Cu surface comprises a thickness range of approximately 50 Å to approximately 70 Å, and
wherein said Cu-Zn alloy fill comprises a thickness range of approximately 300 Å to approximately 700 Å.

Therefore, the Applicants respectfully request that the Examiner's grounds for rejection on this basis be withdrawn.

III. Rejection of Claim 20 on the Grounds of Double Patenting

The Examiner has rejected Claim 20 under the judicially created doctrine of obviousness -type double patenting as being unpatentable over Claim 1 of US 6,515,368. Claim 20 is not herein amended. In US 6,515,368, Claim 1 recites **a *Cu-Zn alloy layer as a thin film layer 30*,** as shown in Exhibit G, that is formed **between** the Cu-fill 26 and the optional layer 20. In contrast, the present invention Claim 20 recites **a *Cu-Zn alloy fill* 30 is the dual-inlaid interconnect structure** as shown in Exhibit F.

Thus, US 6,515,368 does not teach, motivate, nor suggest the present invention Claim 20 reciting:

20. **(original)** A semiconductor device, having a first interim reduced-oxygen copper-zinc (Cu-Zn) alloy fill formed on a copper (Cu) surface and a second interim reduced-oxygen Cu-Zn alloy fill formed on a Cu-fill, both films being formed by electroplating the Cu surface and the Cu-fill, respectively, in a chemical solution, comprising:
a semiconductor substrate having a via; and
an encapsulated dual-inlaid interconnect structure formed and disposed in said via, said interconnect structure comprising:
at least one Cu surface formed in said via;
a first interim reduced-oxygen Cu-Zn alloy fill formed and disposed on the at least one Cu surface;
a Cu-fill formed and disposed on said interim reduced-oxygen Cu-Zn alloy fill; and
a second interim reduced-oxygen Cu-Zn alloy fill formed and disposed on the Cu-fill.

Therefore, the Applicants respectfully request that the Examiner's grounds for rejection on this basis be withdrawn.

CONCLUSION

Accordingly, the Specification, paragraph [0001], and the independent Claims 1, 6, 11, and 16 have been herein amended, and Claims 5 and 15 are canceled, without prejudice, to better encompass the full scope and breadth of the present invention, notwithstanding the Applicants' belief that application would had been allowable as originally filed. The proposed amendments to the Specification and the claims are believed to be fully supported by the originally filed Specification. For all the above advanced reasons, Applicants respectfully submit the application is in condition for allowance. Therefore, favorable consideration of the foregoing proposed amendment and remarks is kindly requested. ***The Examiner is further cordially invited to telephone the undersigned for any reason which would advance the pending claims to allowance.***

Respectfully submitted,

Robert Edward Kasody
Reg. No. 50,268

REK/sf
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LARIVIERE, GRUBMAN & PAYNE, LLP
Post Office Box 3140
Monterey, CA 93942
(831) 649-8800